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MNOS BORAM
MANUFACTURING METHODS
AND TECHNOLOGY PROJECT

Fifth Quarterly Progress Report
1 July 1977 to 31 December 1977

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Contract DAAB07-76-C-0048
WESTINGHOUSE DEFENSE AND ELECTRONIC SYSTEMS CENTER
Systems Development Division
Baltimore, Maryland 21203

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A manufacturing methods project has been initiated to establish a pilot production line for metal nitride oxide semiconductor (MNOS) block oriented random access memory (BORAM) multichip hybrid circuits. During the past reporting period the project has focused on definition of tests, development of test equipment and preparation of test programs.

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TECHNICAL REPORT

MNOS BORAM MANUFACTURING METHODS AND TECHNOLOGY PROJECT

Fifth Quarterly Progress Report

1 July 1977 to 31 December 1977

Prepared by

J.E. Brewer

PROJECT OBJECTIVE: Establish a production capability for metal nitride oxide semiconductor (MNOS) integrated circuits for block oriented random access memory (BORAM).

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Contract DAAB07-76-C-0048

WESTINGHOUSE DEFENSE AND ELECTRONIC SYSTEMS CENTER
Systems Development Division
Baltimore, Maryland 21203

ABSTRACT

A manufacturing methods project has been initiated to establish a pilot production line for metal-nitride-oxide semiconductor (MNOS) block-oriented random-access memory (BORAM) multichip hybrid circuits. During the past reporting period the project has focused on definition of tests, development of test equipment and preparation of test programs.

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PURPOSE

The purpose of manufacturing methods and technology (MM&T) project number 2769758 is to establish a production capability for metal-nitride-oxide semiconductor (MNOS) integrated circuits for block-oriented random-access memory (BORAM).

Military organizations are faced with a difficult hardware problem in the use of modern day computers. A suitable militarized secondary storage technology simply does not exist. Drums and discs cannot stand up under the stress of the ground mobile environment. Military real time programs are forced to be resident in main memory because electromechanical storage access delays cannot be tolerated.

MNOS BORAM holds considerable promise of meeting the military's secondary storage needs. An advanced development Army/Navy MNOS BORAM module has proven that significant volume, weight, power and use flexibility advantages can be achieved. When compared to fixed-head electromechanical storage MNOS BORAM offers MTBF's 10 times longer, and access times above 500 times faster.

This MM&T project will establish for the government a source of supply for MNOS BORAM secondary storage. A pilot production line with a demonstrated capacity of 1,875 hybrid circuit per month will be established. Each hybrid circuit will contain 16 MNOS BORAM integrated circuits. This production rate will provide sufficient hybrid circuits to allow fabrication of three 16.8 megabit BORAM modules per month. The hybrid circuits will conform to Electronics Command Technical Requirement SCS503, and the MM&T project will be conducted in accord with Electronics Command Industrial Preparedness Procurement Requirement Number 15.

1. NARRATIVE AND DATA

Electrical testing and test development has been the area of focused activity during the reporting period. This report describes some of the test capability which has been established to support BORAM hybrid circuit production.

1.1 HYBRID CIRCUIT FUNCTIONAL TEST

A functional test station has been established to process the BORAM memory microcircuit. This test system provides both manufacturing and engineering oriented reports, and is capable of volume throughput in excess of the MM&T production rate requirement.

This report explains the requirements and objectives of the test station development effort, describes the hardware and software which has been developed, gives the functional test specification, and presents data to show that development objectives were achieved.

1.1.1 <u>Statement of the Development Problem</u>

The functional test station must provide specific data in a timely manner in a convenient format. It must with a high confidence level isolate defective chips. In addition, it must comply with the MM&T contract throughput requirement. This discussion will present those detailed requirements.

1.1.1.1 Functional Test Station Purpose

As shown in figure 1-1, the BORAM Memory Microcircuit contains 16 MNOS chips. Figure 1-2 shows the production processing sequence for hybrid circuit assembly and test. The first electrical test after assembly occurs at operation 10, work station A10. Station A10 is the "Hybrid Circuit Functional Test Station". It is located in the MNOS Test Laboratory at the Westinghouse Advanced Technology Laboratories facility.
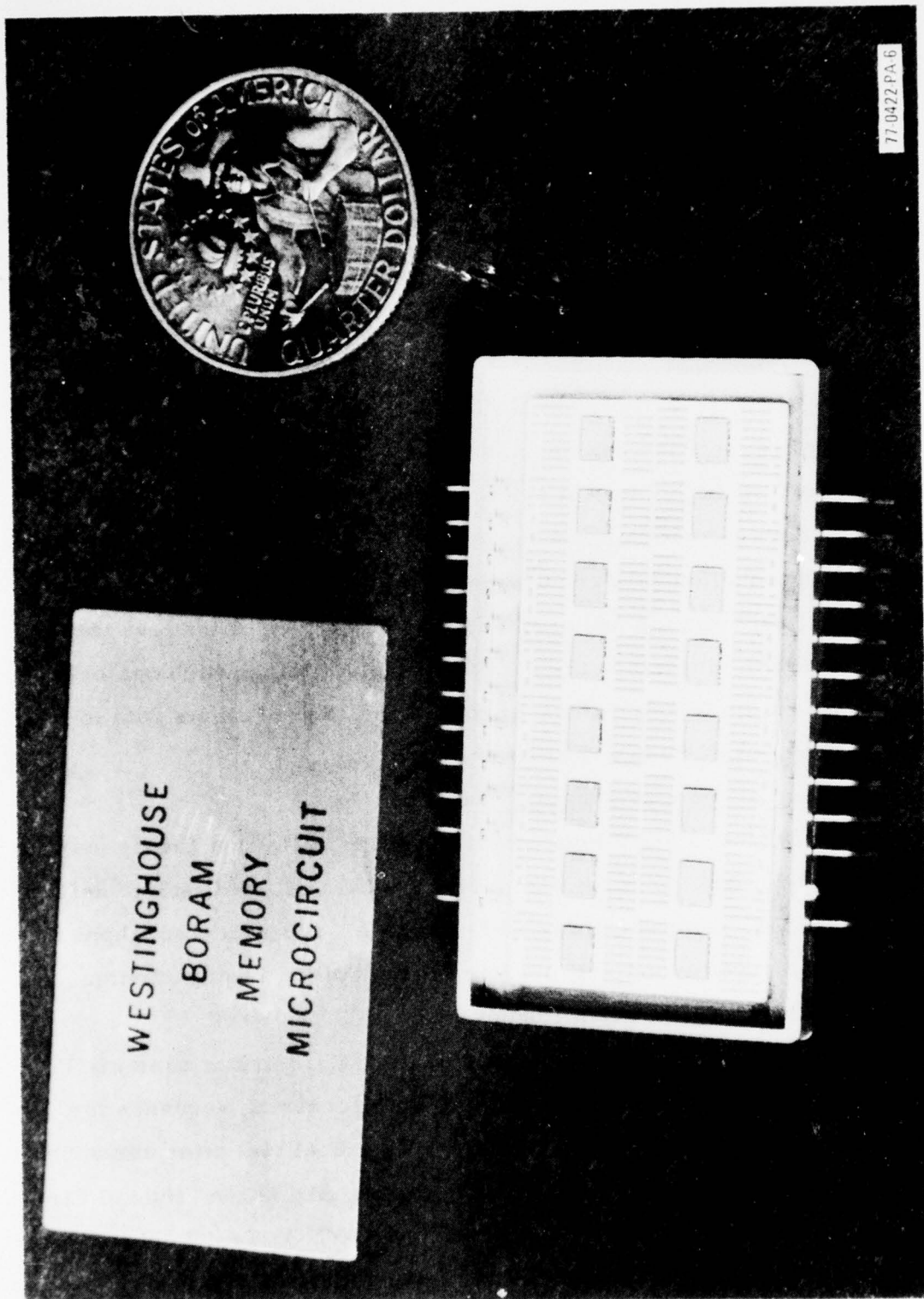
Figure 1-1. BORAM Memory Microcircuit Westinghouse Part 647R527G01
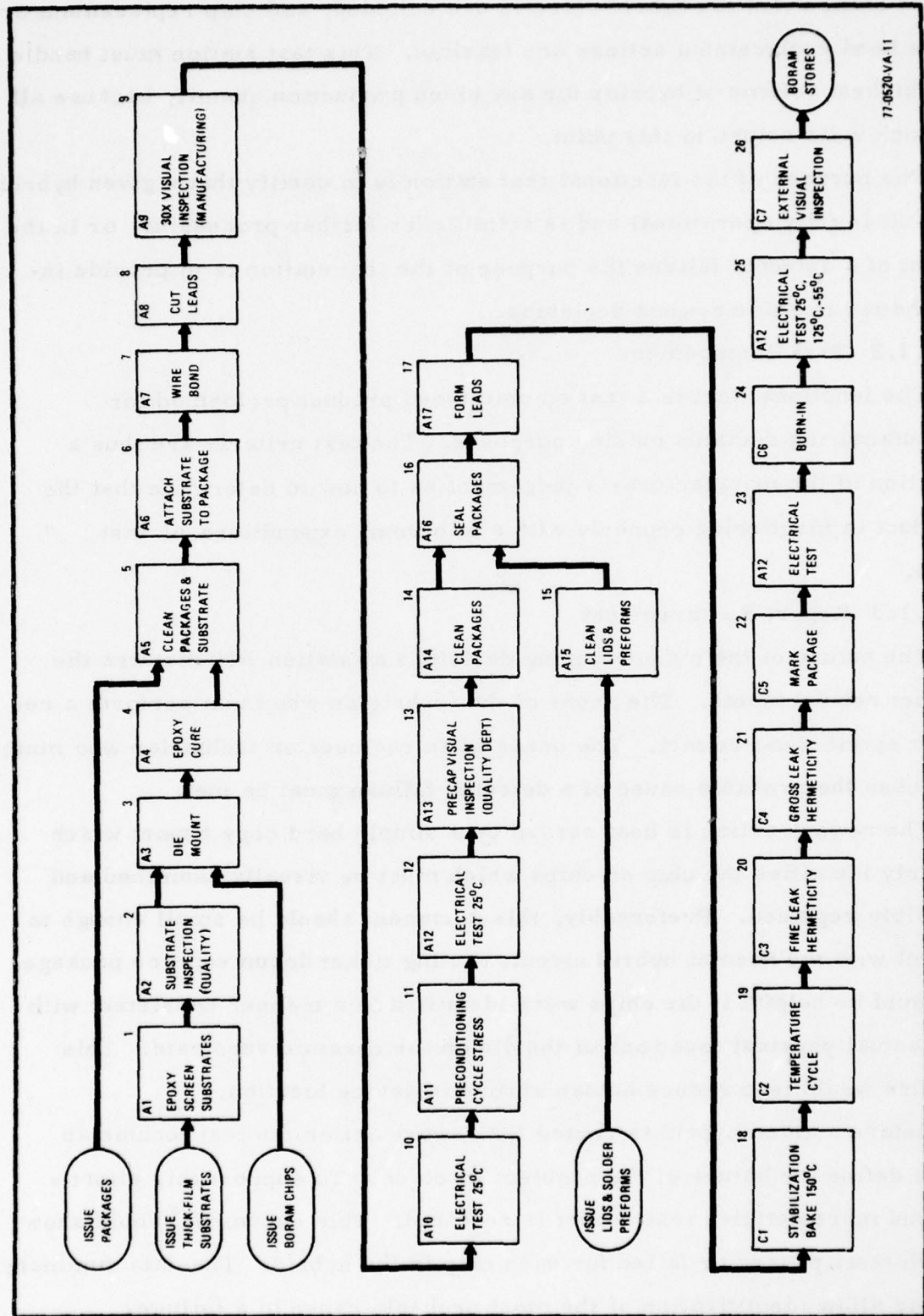
Figure 1-2. MNOS BORAM Hybrid Production Processing Sequence

77-0520-VA-11

At station A10 the hybrid circuits are unlidded, and chip replacement or wire bond replacement actions are feasible. This test station must handle the highest volume of hybrids for any given production quantity because all rework units return to this point.

The purpose of the functional test station is to certify that a given hybrid circuit is fully operational and is suitable for further processing, or in the event of a detected failure the purpose of the test station is to provide information to guide rework decisions.

1.1.1.2 Test Requirement

The functional test is a test on unfinished product performed for manufacturing decision making purposes. The test criteria are thus a function of the manufacturer's judgement as to how to determine that the product is functioning properly with a minimum expenditure of test time.

1.1.1.3 Report Requirements

The nature of the manufacturing decisions at station A10 dictates the report requirements. The needs of the technician who must perform a rework action must be met. The needs of an engineer or technician who must diagnose the probable cause of a detected failure must be met.

The rework action is best served by a simple hard copy report which clearly identifies the chip or chips which must be visually examined and possibly replaced. Preferrably, this document should be small enough to travel with the normal hybrid circuit routing ticket documentation package. It would be helpful if the chips were identified in a manner consistent with the actual physical locations of the die on the ceramic substrate. This feature would tend reduce human errors in device location.

Before a given hybrid is routed for rework action the test technician must define the nature of the problem involved. To support this effort a second more detailed test report is required. This document should show which tests passed or failed for each chip in the hybrid. The data summary should allow identification of the most probable cause of a failure.

1-4

1.1.1.4 Throughput Requirement

The throughput requirement for station A10 is derived from the MM&T contract requirement for pilot line capacity. If the line is operated 5 days a week on a one shift basis, the total volume capacity is required to be at least 1875 hybrids per month.

To examine individual station throughput requirements, it is convenient to express the rate specification in hybrids per hour. A nominal month by the above operating criteria contains 160 hours. Therefore, the line rate requirement is 11.7 hybrids per hour.

Per the production flow diagram, the functional test station must process every hybrid circuit at least one time. Although it is not shown on the flow diagram, the functional test will be repeated again after operation 11. Devices which pass this test will move to the more time consuming test which is operation 12 at station A12. In addition to these two tests per hybrid, any rework action implies two additional tests per hybrid.

An exact computation of the volume which must move through station A10 depends on the amount of rework, and is a complex calculation. A simplified worst case calculation can be made to set upper bounds on the necessary capacity. Arbitrarily assume a very poor rework experience. Say that every hybrid must be reworked 1 time, that 40 percent must be reworked twice, that 20 percent must be reworked three times, and that 5 percent must be reworked four times. The implied number of functional tests per delivered finished hybrid are:

   2 tests (1 initial + 1 rework + 0.4 rework + 0.2 rework + 0.05 rework)

   2 tests (2.65)

   5.30 tests

Since the required rate of finished hybrids is 11.7 per hour, the upper bound capacity of station A10 to meet contract requirements is:

   5.30 x 11.7 hybrids/hour

   62 hybrids/hour

1.1.1.5 Additional Objectives

This report is primarily concerned with the rapid screening of the BORAM hybrid at operation 10 in the hybrid assembly and test flow. There are, however, test considerations of importance to BORAM production which are beyond the scope of operation 10; and yet should influence the design of the test system.

The production of BORAM systems involves memory testing at four levels of product complexity:

    a. Memory Chips

    b. Multichip Hybrids

    c. Memory Cards or Modules

    d. Memory Systems

These tests are very similar. It would be a major advantage if the test system designed for hybrid test could also conveniently perform the other three levels of test.

Finally the test system design must consider the practical aspects common to all equipment developments. Hardware cost and reliability must be reasonable. Software development and documentation must be easily accomplished without major labor expenditures.

1.1.2 Functional Test Station Description

The BORAM Functional Test Station is based on an architectural concept which contributes greatly to economy and ease of use. The system is suitable for application to all four levels of BORAM testing. This discussion explains the design concept, describes the hardware, reviews the hardware operation, examines the software functions, and briefly describes the microcode assembler used to support software development.

1.1.2.1 Macrolevel and Microlevel Partitioning

The fundamental architectural concept on which the design of the Functional Test Station is based is to partition the test problem into two parts: a "macrolevel" and a "microlevel". Figure 1-3 illustrates the points of concern for each level.

MICROLEVEL

Elementary Control Signals

- Signal Sequences
- Pattern Generation
- Data Comparison
- I/O Drivers and Buffers

Device Under Test

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MACROLEVEL

Test Sequence Control

- Operator Interaction
- Test Flow Logic
- Report Generation
- Information Storage

Operator

Report Printer

Program and Data Storage Element
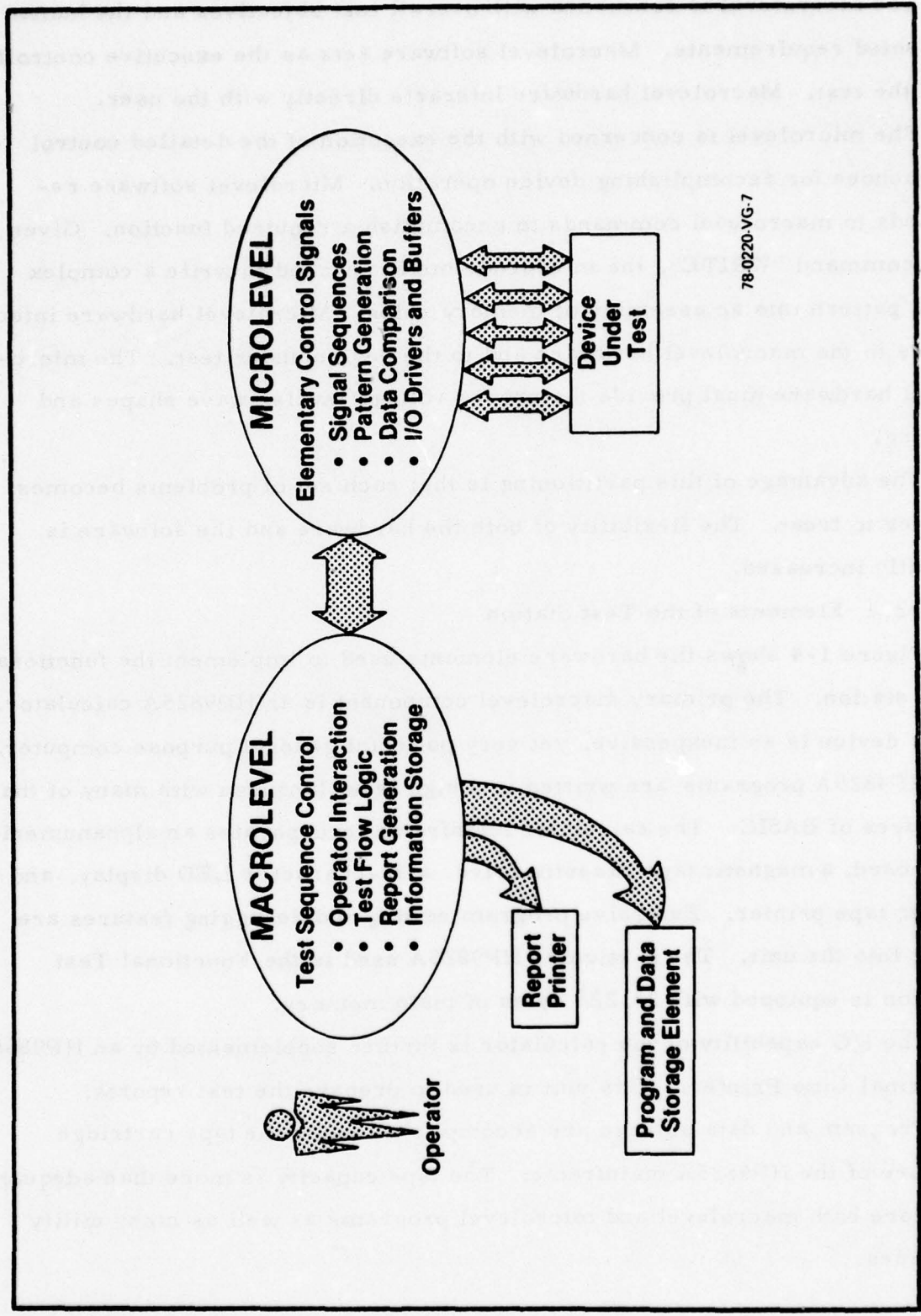
Figure 1-3. Test System Functional Block Diagram

The macrolevel is concerned with overall test objectives and the human oriented requirements. Macrolevel software acts as the executive controller for the test. Macrolevel hardware interacts directly with the user.

The microlevel is concerned with the execution of the detailed control sequences for accomplishing device operation. Microlevel software responds to macrolevel commands to accomplish a required function. Given the command "WRITE", the microcode might proceed to write a complex data pattern into an assembly of memory chips. Microlevel hardware interfaces to the macrolevel hardware and to the device under test. The microlevel hardware must provide the proper voltage levels, wave shapes and timing.

The advantage of this partitioning is that each set of problems becomes easier to treat. The flexibility of both the hardware and the software is greatly increased.

1.1.2.2 Elements of the Test Station

Figure 1-4 shows the hardware elements used to implement the functional test station. The primary macrolevel component is an HP9825A calculator. This device is an inexpensive, yet very powerful general purpose computer.

HP9825A programs are written in a high level language with many of the features of BASIC. The calculator mainframe incorporates an alphanumeric keyboard, a magnetic tape cassette drive, a 32-character LED display, and a paper tape printer. Extensive program editing and debugging features are built into the unit. The particular HP9825A used in the Functional Test Station is equipped with 23, 228 bytes of main memory.

The I/O capability of the calculator is further supplemented by an HP9866B, Thermal Line Printer. This unit is used to prepare the test reports.

Program and data storage are accomplished using the tape cartridge feature of the HP9825A mainframe. The tape capacity is more than adequate to store both macrolevel and microlevel programs as well as many utility routines.

1-8
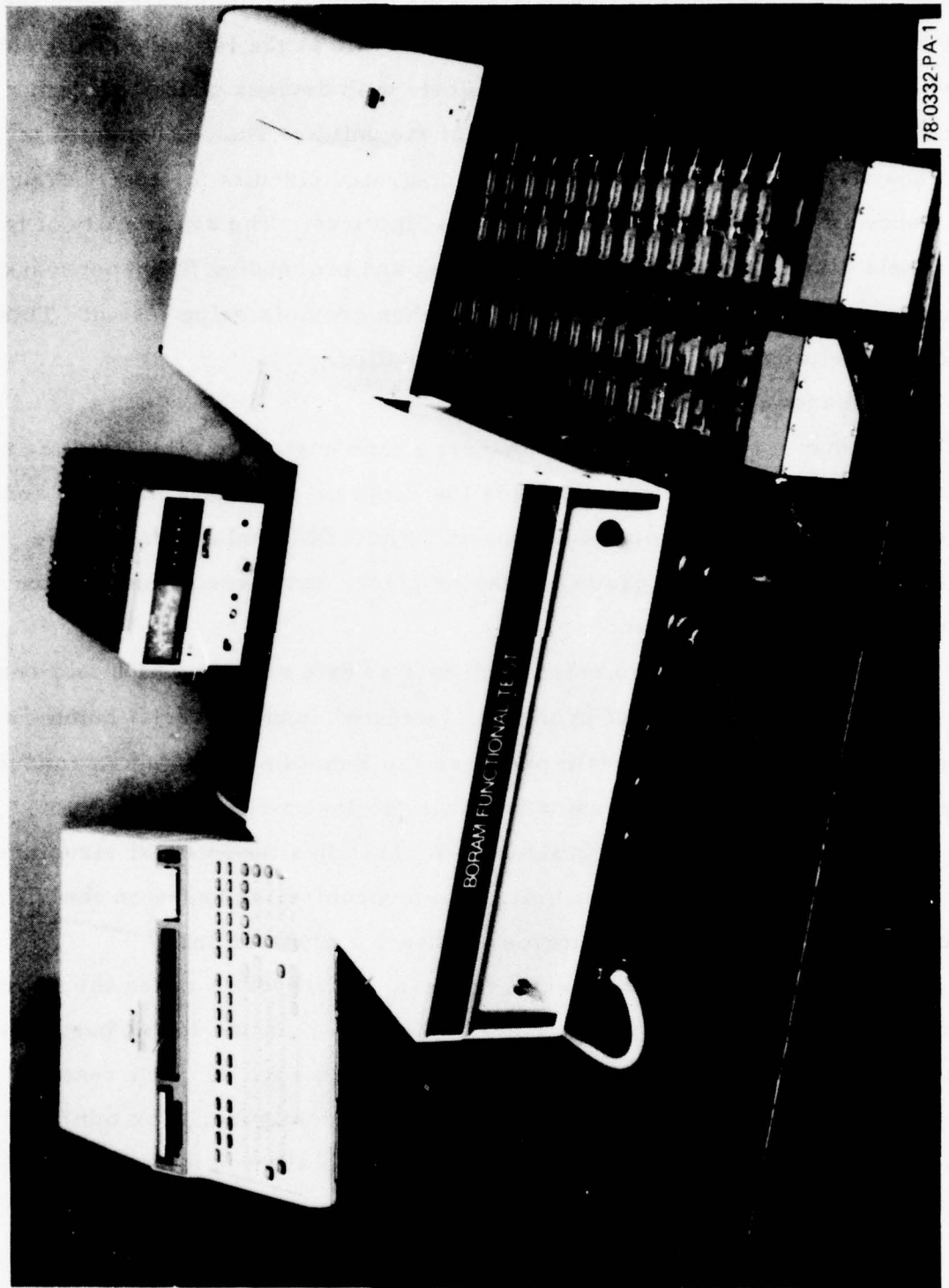
Figure 1-4. Elements of the BORAM Functional Test Station

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1-9

The microlevel component in the system is the BORAM Function Test Unit shown in the foreground of figure 1-4. This device communicates with the HP9825A via a 16-bit channel. This is the cable at the left side of the unit. Two channels are provided to communicate with devices under test. In figure 1-4, the two cables at the right of the unit are shown connected to PC boards which can accommodate 30 integrated circuits for test. Figure 1-5 shows the BORAM hybrid circuit test fixtures. The availability of two channels allows the operator to be loading and processing the paper work for one group of eight hybrids while the other group is being tested. This provision eliminates time losses due to handling.

1.1.2.3 Hardware Operation

To conduct a test the operator inserts a tape cartridge containing the test program into the HP9825A. He loads the program into main memory and presses the RUN button on the keyboard. The LED display informs the operator as to what processes are taking place, and gives prompts when operator action is required.

The operator is asked to enter such data as date of test, which test channel is to be used, the number of hybrids to be tested, and the serial numbers of each hybrid. The test program prepares the Function Test Unit to conduct the microfunctions by communicating over the 16-bit channel.

The block diagram shown in figure 1-6 describes the internal structure of the BORAM Functional Test Unit. A microcontroller based on the Am2911 microsequencer chip forms the heart of the test unit.

During the initialization phase of the test, the HP9825A reads the micro-code program from the tape cartridge and sends it via the 16-bit bus to the Functional Test Unit. The microcode is stored in a RAM. This feature makes the unit particularly easy to use and to reconfigure. The option of microcode storage in ROM's or PROM's was also allowed for in the hardware design.

Figure 1-5. BORAM Hybrid Circuits in Functional Test Fixture
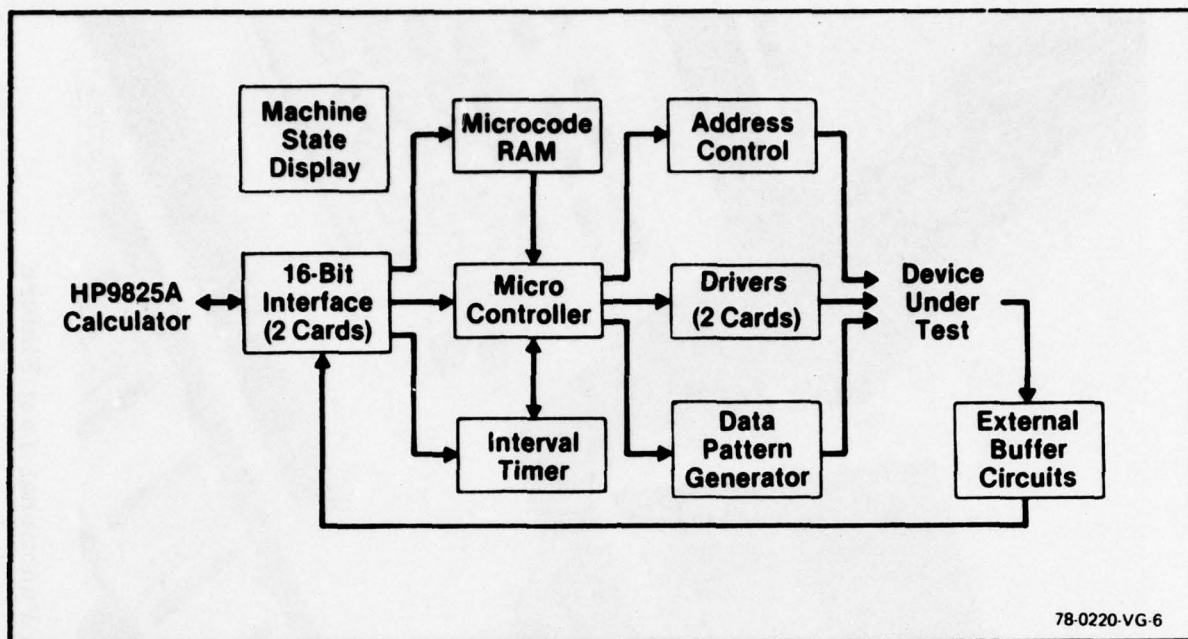
Figure 1-6. BORAM Functional Test Unit

The interface to the device under test necessarily involves specific wave-shapes and voltage levels. The output circuits on the driver cards, the address card and the data pattern card accomplish this function.

Pulse timing and duration are set by the microcode routines or by command from the HP9825A. For example, the erase and write times for BORAM chips are set by calculator software.

Data patterns and data checking are selected by HP9825A software. The data pattern generator card in the Functional Test Unit provides the selected patterns.

One feature of some importance is not shown clearly in figure 1-6. The buffered data coming from the device under test is actually routed back to the data pattern generator card. On that card the 16 signals can be exclusive ORed with the source data pattern. Thus, the HP9825A can command that the Functional Test Unit return either the data pattern read from the device under test, or the error pattern resulting from the exclusive OR operation.

1-12

After initialization is complete the HP9825A LED display will indicate "READY FOR TEST". When the operator pushes the "CONTINUE" button, the test sequence for up to eight hybrid circuits will be automatically conducted. At the conclusion of the test, production oriented reports will be printed for each hybrid circuit. Then an engineering oriented report will be printed for all of the hybrids under test.

1.1.2.4 Software Considerations

For operation the Functional Test Station requires two sets of software programs. Figure 1-7 gives an overview of the programming task. The macrolevel program runs on the HP9825A. The microlevel program runs on the microcontroller in the Functional Test Unit.

The software development begins with a clear statement of test objectives. What is it that must be achieved? The macro planning activity extends these requirements into specific definitions of the test sequence and output reports. Then the desired tests are detailed in terms of tape file storage, main memory variable assignments, and operator interaction requirements. Finally the actual coding can be performed.

Figure 1-8 is a sample of the HP9825A coding used in the BORAM Hybrid Test Program. The HP9825A has a wide range of instruction types. For example, it provides string operations, matrix operations, binary operations, and all the usual features of BASIC. In addition, it offers a rich assortment of instructions to control and to interact with I/O devices.

The microcode development task begins with a careful definition of the interface to the device under test. What are the required signals, and how do they relate in time sequence to accomplish specific functions. What are the functions that the macrocode will request? How should the addressing sequence be arranged?

The microcoding task cannot really be separated from hardware design. The criteria for proper program operation is the actual observation of the waveforms at the terminals of the device under test.
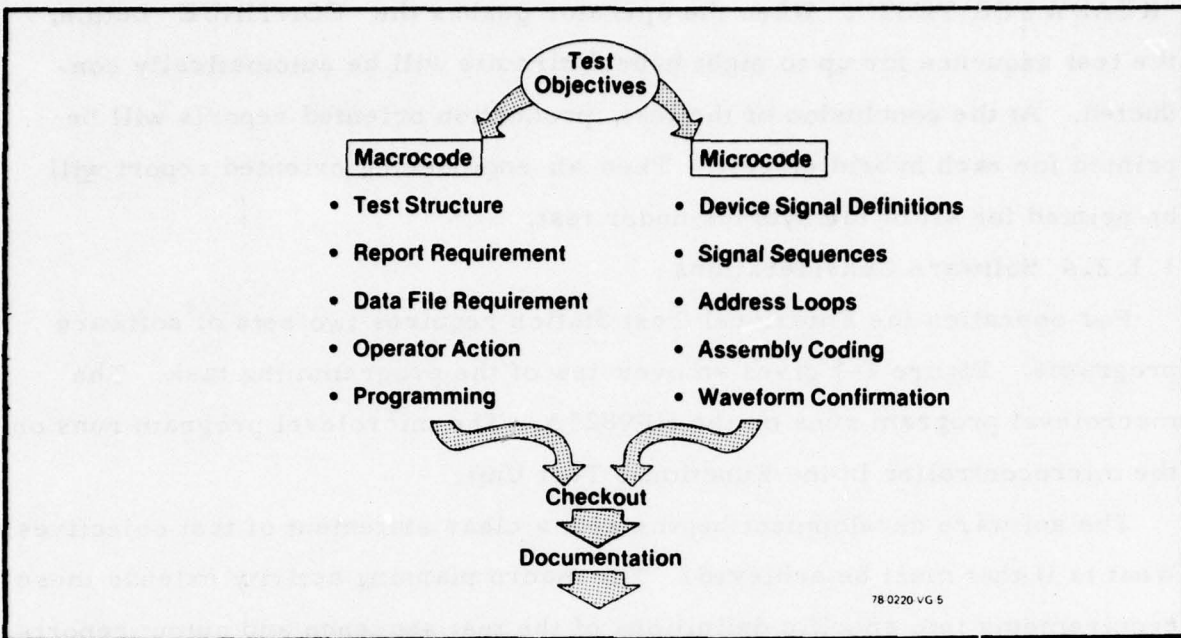
Figure 1-7. Software Development Considerations

Microcode development depends heavily on the use of the HP9825A. An assembler and various utility routines allow the engineer to interactively observe the effects at the device under test and modify this program until the desired results are achieved.

1.1.2.5 Microcode Assembler

The primary tool used for microcode development is an assembly program. The assembly language instruction set is presented in table 1-1. The mnemonics were established by Advanced Micro Devices, Inc which manufacturers the Am2911 microsequencer chip.

The assembler allows the engineer to key in lines of code at the HP9825A keyboard. The code and any arguements are examined for consistency with validated symbols and instruction formats. If an error is detected, the assembler asks for re-entry of the line. When the code is accepted as valid it is written into a microcode memory map file on the tape cartridge.

```
201: "TEST SUBROUTINES":
202: "SP":eir 8,162;wtb 8,21;ret
203: "TS1":eir 8,162;wtb 8,21;ret
204: "TS2":wtb 8,C;wait 1
205: if rds(8)mod2=0;jmp 0
206: "TS4":wtb 8,C-8;eir 8,130
207: for I=0 to 7;-1→Y;tfr 8,"XX",2048
208: if rds("XX")=-1;jmp 0
209: for J=1 to 2048;band(rdb("XX"),Y)→Y;next J
210: band(Y→X[W,I],X[7,I])→X[7,I];next I
211: wrt 16.7,"TEST ",W;ret
212: "TS3":for I=0 to 7;wrt 16.9,I+1,X[W,I];next I;spc ;ret
213: "################":
214: prt "BORAM HYBRID","TEST PROGRAM";fmt 9,'PAIR ",f1.0,x,f8.0
215: "D1":ent "Test Channel A or B?",A$
216: if pos(A$," ")=1;A$[2]→A$;jmp 0
217: 0→C;if "A"=A$[1,1];18→C
218: if "B"=A$[1,1];16→C
219: if C=0;prt "INVALID INPUT";gto "D1"
220: if rds(8)<299;dsp "TURN ON TEST SYSTEM";jmp 0
221: wait 10;dsp "NOW LOADING MICROCODE";wtc 8,32
222: for I=0 to 255;num(C$[I+1,1,1])-48→K;if K>15;K-7→K
223: wtc 8,1;wtb 8,16I+K;0→L
224: for J=2 to 5;num(C$[I+1,J,J])-48→K;if K>5;K-7→K
225: 16L+K→L;next J;if L>32767;L-65536→L
226: wtc 8,3;wtb 8,L;next I
227: dsp "LOADING DATA RAM";buf "XX"
228: for J=1 to 4;for I=1 to 128;wtb "XX",I;next I;next J;gsb "SP"
229: wtb 8,1024;wtb 8,4;tfr."XX",8;wait 1
230: if rds("XX")=-1;jmp 0
231: eir 8,0;wait 10;eir 8,162;fmt 8,f2.0,x,ft.0,x,f6.0
232: "CLEAR TIME":1000→T;wtb 8,0;wtb 8,int((T-1)/2)
233: "WRITE TIME":200→U;wtb 8,13;wtb 8,int((U-10)/2)
234: "TEST":ent "HOW MANY MICROCIRCUITS?",O
235: spc ;prt "ENTER HYBRID";prt "SERIAL NUMBERS";spc ;spc
236: for I=1 to O;ent S[I];next I
237: dsp "READY FOR TEST";stp
238: for I=1 to 7;for J=0 to 7;-1→X[I,J];next J;next I
239: fmt 8,f2.0,x,f6.0,x,f6.0;fmt 9,"PAIR ",f1.0,"=",f6.0
240: fmt 7,c5,f1.0;fxd 0
241: "#1":dsp "PERFORMING TEST #1";buf "XX";1→W;gsb "TS1"
242: wtb 8,3072;gsb "TS2"
243: prt "COUNTER";gsb "TS3"
244: "#2":dsp "PERFORMING TEST #2";2→W;buf "XX";gsb "SP"
245: wtb 8,392
246: for I=1 to 10;wtb 8,C;wait 1
247: if rds(8)mod2=0;jmp 0
248: next I;gsb "TS1"
249: wtb 8,2696;gsb "TS2"
250: prt "ERASE RECOVERY";prt "CHECKER BD";gsb "TS3"
*10809
```

Figure 1-8. Sample of Macrocode for the Hybrid Test Program

TABLE 1-1

MICROCODE ASSEMBLY LANGUAGE INSTRUCTION SET

Mnemonic	I_3	I_2	I_1	I_0	Instruction
JZ	L	L	L	L	Jump to Address Zero
CJS	L	L	L	H	Conditional Jump-to-Subroutine with Jump Address in Pipeline Register
JMAP	L	L	H	L	Jump to Address at Mapping PROM Output
CJP	L	L	H	H	Conditional Jump to Address in Pipeline Register
PUSH	L	H	L	L	Push Stack and Conditionally Load Counter
JSRP	L	H	L	H	Jump-to-Subroutine with Starting Address Conditionally Selected from Am2911 R-Register or Pipeline Register
CJV	L	H	H	L	Conditional Jump to Vector Address
JRP	L	H	H	H	Jump to Address Conditionally Selected from Am2911 R-Register or Pipeline Register
RFCT	H	L	L	L	Repeat Loop if Counter is not Equal to Zero
RPCT	H	L	L	H	Repeat Pipeline Address if Counter is not Equal to Zero
CRTN	H	L	H	L	Conditional Return-from-Subroutine
CJPP	H	L	H	H	Conditional Jump to Pipeline Address and Pop Stack
LDCT	H	H	L	L	Load Counter and Continue
LOOP	H	H	L	H	Test End of Loop
CONT	H	H	H	L	Continue to Next Address
JP	H	H	H	H	Jump to Pipeline Register Address

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At anytime the engineer may examine lines of code on the LED display or he may request a hard copy memory map listing. Figure 1-9 is an example of such a listing. The address space ranges from 000 to 255. The map shows the assembly language instruction and arguments, and then gives the equivalent data as it will appear in the LED display (machine state display per figure 1-6) incorporated in the Functional Test Unit. These seven hexadecimal characters are convenient for confirming that the hardware has actually received the desired code.

1.1.3 Functional Test Station Performance

The BORAM Functional Test Station is fully operational, and has been used to test groups of hybrid circuits. This discussion reviews the observed characteristics of the test station in such a manner that judgements can be made as to whether development objectives have been achieved.

```
MICROCODE ASSEMBLY LANGUAGE MEMORY MAP

RAM        INST  FIELD  FIELD  FIELD  FIELD  LED DISPLAY
ADDRESS    CODE  ONE    TWO    THREE  FOUR   ON HARDWARE

128        LDCT  4065                        80 C 0FE1
129        CONT  -P39   -TM1   -P12   PH1    81 E 0001
130        CONT  -P39   -TM1   -P12   PH2    82 E 0002
131        CONT  -P39   -TM1   -P12   P04    83 E 0000

132        CJS   252    -GND                 84 1 F000
133        CJS   247    -GND                 85 1 F700
134        RPCT  129    CTR                   86 9 811F
135        CRTN         -GND                  87 A 0300

136        CONT  -P39   AMR    -P12   P04    88 E 0300
137        CONT  -P39   -AMR   -P12   P04    89 E 0500
138        CRTN         -GND                  8A A 0000
139        CONT  -P39   -TM1   -P12   P04    8B E 0000

140        CONT  -P39   -TM1   -P12   GCP    8C E 0007
141        CRTN         -GND                  8D A 0000
142        LDCT  4095                         8E C 0FFF
143        RPCT  143    CTR                   8F 9 8F1F

144        CRTN         -GND                  90 A 0000
145        JZ                                 91 0 0000
146        CONT  -ST0   -BPE   -P12   P04    92 E 2400
147        CONT  -P39   -TM1   CLL    F04    93 E 0600

148        CONT  -P39   -TM1   -CSB   P04    94 E 0070
149        CONT  -FLG   -TM1   -CSA   P04    95 E 7060
150        CRTN         -GND                  96 A 0000
151        JZ                                 97 0 0000

152        CONT  -P39   -CEP   -P12   P04    98 E 0500
153        CONT  -P39   BCE    -P12   P04    99 E 0F00
154        CONT  -P39   -TM1   -F12   ACP    9A E 0004
155        CONT  -P39   -BCE   -P12   P04    9B E 0700

156        CONT  -P39   CEP    -P12   P04    9C E 0D00
157        CRTN         -GND                  9D H 0000
158        JZ                                 9E 0 0000
159        JZ                                 9F 0 0000
```

SEQ#700000   78-0332-VA-4

Figure 1-9. Sample Microcode Listing

1.1.3.1 Test Sequence

The hybrid circuit under consideration contains 16 of the BORAM 6002 chips. Figure 1-10 shows the functional organization of the 6002 chip. Figures 1-11 and 1-12 provide the circuit diagram of the multi-chip hybrid.

The microcircuit has two data inputs (DWA and DWB) and two data outputs (DRA and DRB). The "A" data lines are associated with the eight odd numbered chips. The "B" data lines are associated with the eight even numbered chips. Each chip select line controls one odd and one even numbered device. Data outputs are tristate. A deselected chip is powered down, and its DR output line is in a high impedance state. In the hybrid circuit only one odd and one even chip may be selected at any given time. The selected chip controls the output bus, and has both active source and sink capability.

Table 1-2 summarizes the six tests performed at the Functional Test Station. The referenced figures and tables document the details of each test (figures 1-13, 1-14 and tables 1-3, 1-4). The counter pattern test
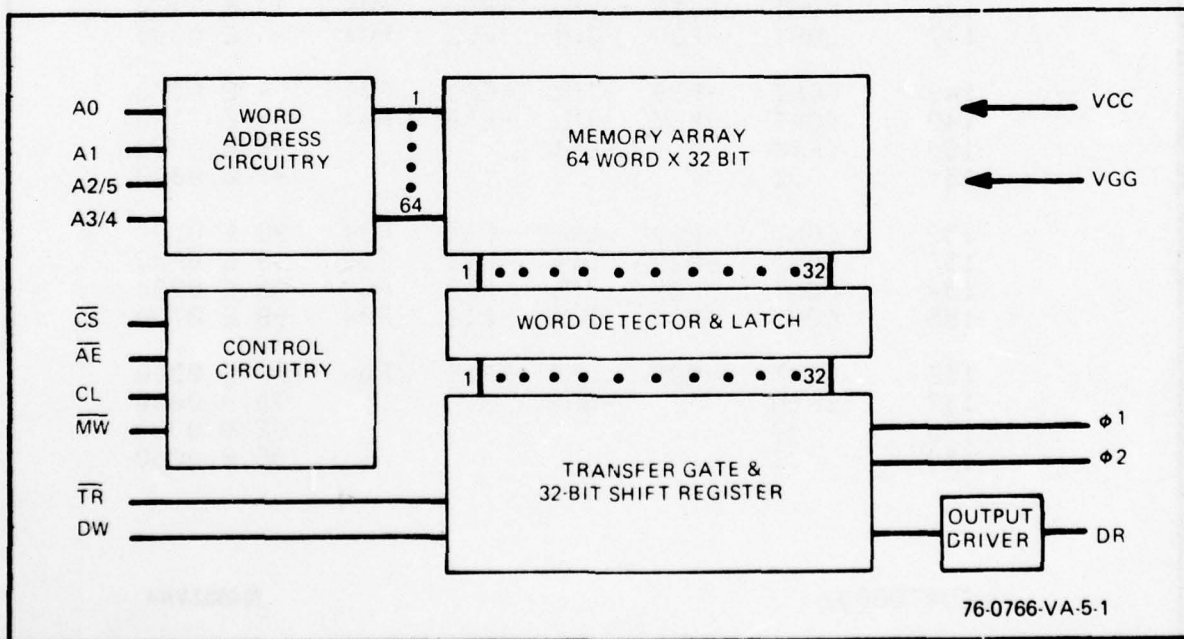
Figure 1-10. BORAM 6002 Functional Block Diagram

1-18
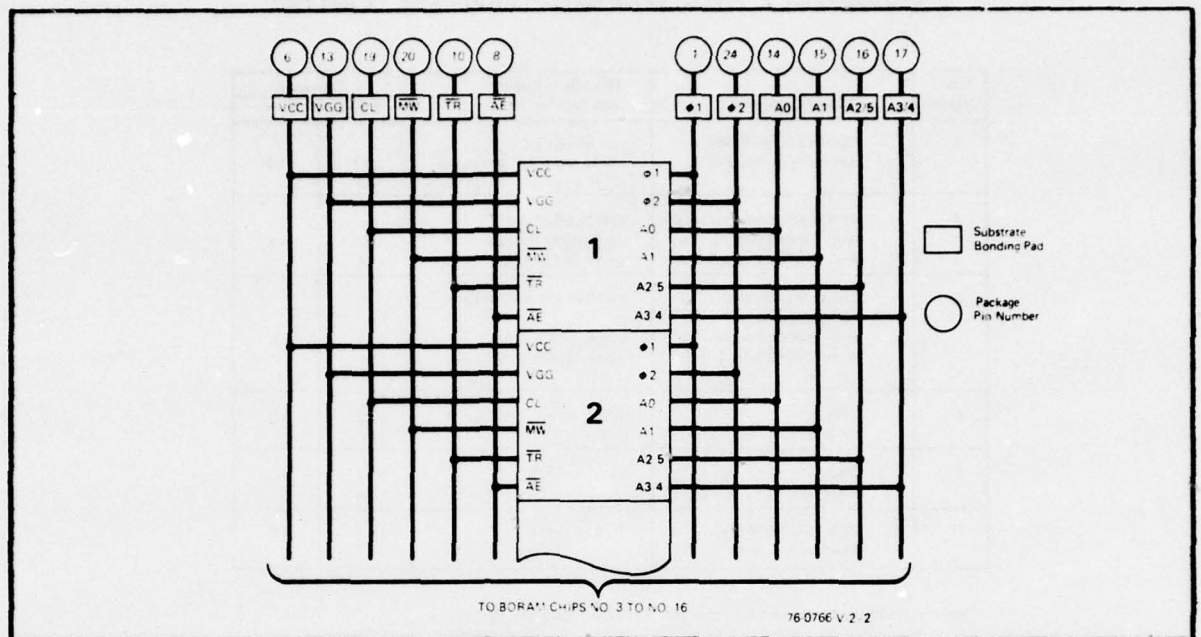
Figure 1-11. Bussed Connections in BORAM Memory Microcircuit
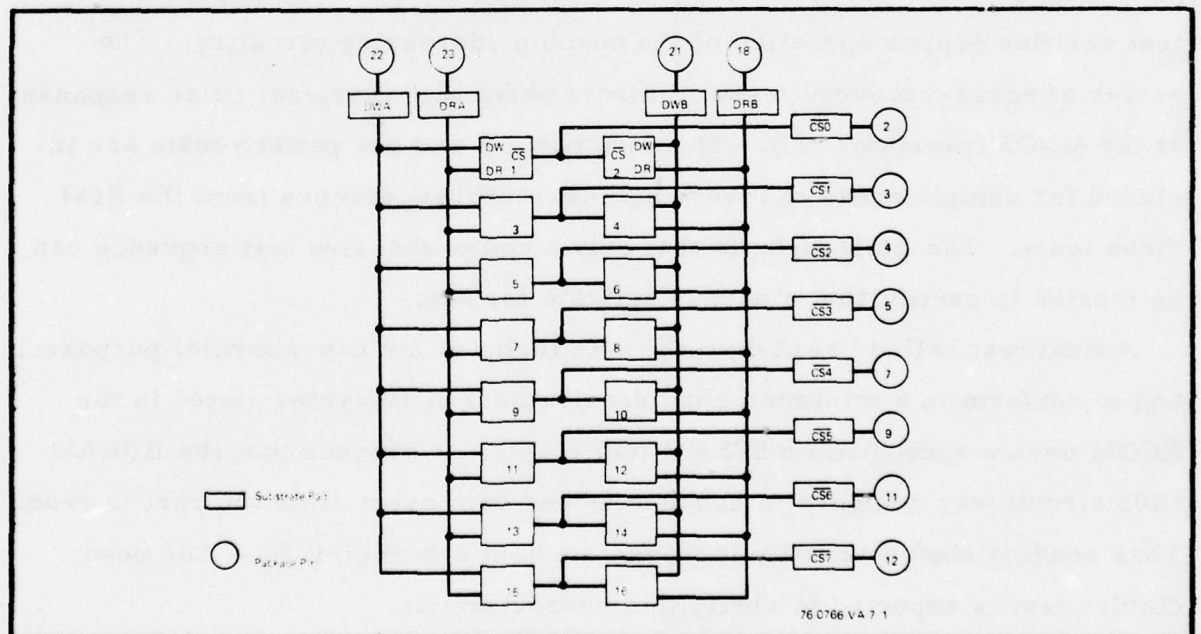
Figure 1-12. BORAM Memory Microcircuit Data I/O and
Chip Select Connections

1-19

TABLE 1-2

SUMMARY AND DESCRIPTION OF TESTS*

Test Number	General Description	32-Bit Shift Register Data Pattern	References	
			Figures	Table
1	COUNTER PATTERN for addressing verification	row address ≡ a MS 16 bits = 2a + 2 in binary LS 16 bits = 2a + 1 in binary	1-13 1-14	1-3
2	ERASE RECOVERY-CHKBD Write CHKBD BAR 10 times Write CHKBD 1 time & read	CHECKER BOARD a even 1010 ~1010 a odd 0101 ~0101	1-13 1-14	1-4
3	ERASE RECOVERY-CHKBD BAR Write CHKBD 9 times Write CHKBD BAR 1 time & read	CHECKERBOARD BAR a even 0101 ~0101 a odd 1010 ~1010	1-13 1-14	1-4
4	ZERO Write ZERO 1 time & read	0000 ~ 0000	1-13 1-14	1-3
5	ONE Write ONE 1 time & read	1111 ~ 1111	1-13 1-14	1-3
6	READ DISTURB-ONE Read device 9 times	1111 ~ 1111	1-13 1-14	1-5

*Nominal supply conditions for all tests are VCC = +15V and VGG = −15V·

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places unique data in every addressable row of the memory chips. This test verifies proper operation of the on-chip addressing circuitry. The series of erase-recovery tests eliminate parts with marginal pulse response at the MNOS transistor cell. The zero pattern and one pattern tests are included for completeness to insure against marginal escapes from the first three tests. The philosophy is that only a comprehensive test sequence can be trusted to certify that a part is suitable for use.

A final test called "read disturb" was included for experimental purposes, and to conform to a minimum read requirement of 10 cycles stated in the ECOM device specification SCS503 (table 1-5). It happens that the BORAM 6002 circuit was designed to enhance stored data every time the part is read. Thus reading should actually increase the data retention time. The read disturb test is expected to verify this characteristic.

1-20
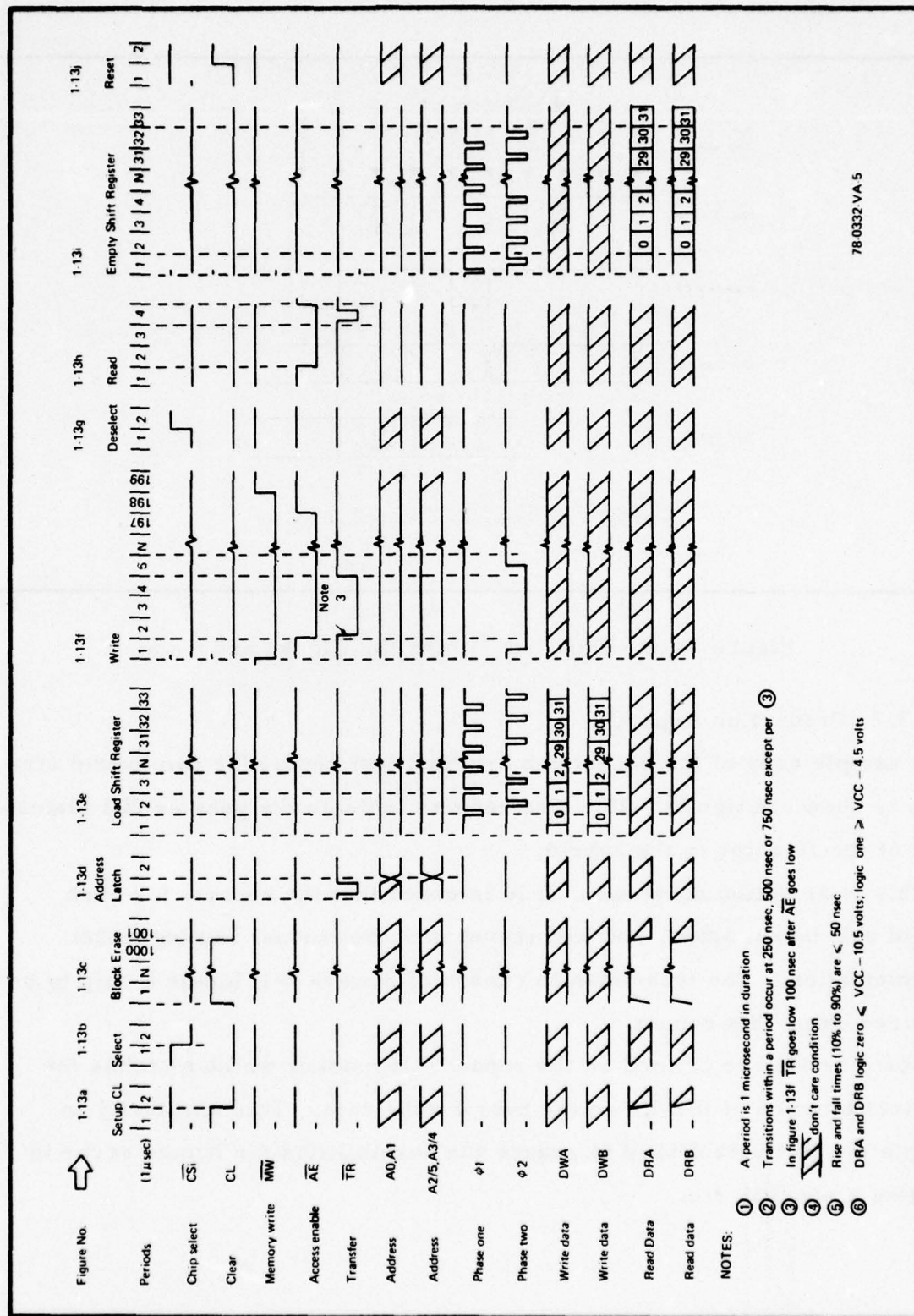
Figure 1-13. Operating Sequences for Functional Tests

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NOTES:

① A period is 1 microsecond in duration

② Transitions within a period occur at 250 nsec, 500 nsec or 750 nsec except per ③

③ In figure 1-13f $\overline{TR}$ goes low 100 nsec after $\overline{AE}$ goes low

④ don't care condition

⑤ Rise and fall times (10% to 90%) are ≤ 50 nsec

⑥ DRA and DRB logic zero ≤ VCC – 10.5 volts; logic one ≥ VCC – 4.5 volts

Figure No.												
		1-13a	1-13b	1-13c	1-13d	1-13e	1-13f	1-13g	1-13h	1-13i	1-13j

Setup CL — Select — Block Erase — Address Latch — Load Shift Register — Write — Deselect — Read — Empty Shift Register — Reset

Periods (1 μsec)

Chip select $\overline{CS}i$

Clear CL

Memory write $\overline{MW}$

Access enable $\overline{AE}$

Transfer $\overline{TR}$

Address A0,A1

Address A2/5, A3/4

Phase one $\phi 1$

Phase two $\phi 2$

Write data DWA

Write data DWB

Read Data DRA

Read data DRB

Note 3

Figure 1-14.   Detailed Timing for Clocks and Data

1.1.3.2 Production Report

A sample copy of the production oriented test report for two hybrid cir-
cuits is shown in figure 1-15. The reports indicate the pass or fail status of
each of the 16 chips in the hybrid.

This is an action document. It is intended that the reports for each
hybrid will be cut apart, and will travel with the normal routing ticket
documentation. The technician in charge of rework will locate a chip to be
repaired using this report.

Test results are printed on the report in a manner which matches the
physical location of the die on the hybrid substrate. This similarity in
orientation was established to reduce the possibilities for human error in
locating a specific die.

1-22

TABLE 1-3

MEMORY TESTS LOGICAL FLOW SEQUENCE

Step	Logical Operation
1	Setup CL per fig. 1-13a
2	Initialize chip select counter (i=0 and $\overline{CSi} = \overline{CS0}$)
3	Setup $\overline{CSi}$ per fig. 1-13b
4	Erase selected chips per fig. 1-13c
5	Initialize address counter (address = 0)
6	Setup address lines per fig. 1-13d
7	Set data pattern per table 1-2
8	Load DWA and DWB shift registers per fig. 1-13e
9	Write data per fig. 1-13f
10	Increment address counter (address = address + 1)
11	If (address < 64) then 6
12	Reset $\overline{CSi}$ per fig. 1-13g
13	Increment chip select counter (i=i+1 and $\overline{CSi} = \overline{CSi+1}$)
14	If (i < 8) then 3
15	Initialize chip select counter (i = 0 and $\overline{CSi} = \overline{CS0}$)
16	Setup $\overline{CSi}$ per fig. 1-13b
17	Initialize address counter (address = 0)
18	Setup address lines per fig. 1-13d
19	Read data to latch per fig. 1-13h
20	Empty DRA and DRB shift registers per fig. 1-13i
21	If (data ≠ (per table 1-2),) then record FAIL
22	Increment address counter (address = address + 1)
23	If (address < 64) then 18
24	Reset $\overline{CSi}$ per fig. 1-13g
25	Increment chip select counter (i = i+1 and $\overline{CSi} = \overline{CSi+1}$)
26	If (i < 8) then 16
27	Reset CL per fig. 1-13j
28	End Routine

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TABLE 1-4

ERASE RECOVERY TESTS LOGICAL FLOW SEQUENCE

Step	Logical Operation
1	Setup CL per fig. 1-13a
2	Initialize write counter (j=0)
3	Initialize chip select counter (i=0 and $\overline{CSi} = \overline{CS0}$)
4	Select $\overline{CSi}$ per fig. 1-13b
5	Erase selected chips per fig. 1-13c
6	Initialize address counter (address = 0)
7	Setup address lines per fig. 1-13d
8	Set data pattern per table 1-2
9	Load DWA and DWB shift registers per fig. 1-13e
10	Write data per fig. 1-13f
11	Increment address counter (Address = Address + 1)
12	If (address <64) then 7
13	Reset $\overline{CSi}$ per fig. 1-13g
14	Increment chip select counter (i = i+1 and $\overline{CSi} = \overline{CSi+1}$)
15	If (i $<$ 8) then 4
16	Increment write counter (j = j+1)
17	If (j $<$11) then 3
18	Initialize chip select counter (i = 0 and $\overline{CSi} = \overline{CS0}$)
19	Select $\overline{CSi}$ per fig. 1-13b
20	Erase selected chips per fig. 1-13c
21	Initialize address counter (address = 0)
22	Setup address lines per fig. 1-13d
23	Setup data pattern (complement of step 8 data)
24	Load DWA and DWB shift registers per fig. 1-13e
25	Write data per fig. 1-13f
26	Increment address counter (address = address +1)
27	If (address <64) then 22
28	Reset $\overline{CSi}$ per fig. 1-13g
29	Increment chip select counter (i=i+1 and $\overline{CSi} = \overline{CSi+1}$)
30	If (i $<$8) then 19
31	Initialize chip select counter (i = 0 and $\overline{CSi} = \overline{CS0}$)
32	Select $\overline{CSi}$ per fig. 1-13b
33	Initialize address counter (address = 0)
34	Setup address lines per fig. 1-13d
35	Read data to latch per fig. 1-13h
36	Empty DRA and DRB shift registers per fig. 1-13i
37	If (data $\neq$ per table 1-2) then record FAIL
38	Increment address counter (address = address +1)
39	If (address <64) then 34
40	Reset $\overline{CSi}$ per fig. 1-13g
41	Increment chip select counter (i = i+1and $\overline{CSi} = \overline{CSi+1}$)
42	If (i $<$8) then 32
43	Reset CL per fig. 1-13j
44	End Routine

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TABLE 1-5

READ DISTURB TEST LOGICAL FLOW SEQUENCE

Step	Logical Operation
1	Setup CL per fig. 1-13a
2	Initialize read loop counter (J=0)
3	Initialize chip select counter (i=0 and $\overline{CSi} = \overline{CS0}$)
4	Setup $\overline{CSi}$ per fig. 1-13b
5	Initialize address counter (address = 0)
6	Setup address lines per fig. 1-13d
7	Read data to latch per fig. 1-13h
8	Empty DRA and DRB shift registers per fig. 1-13i
9	If (data ≠ one) then record FAIL
10	Increment address counter (address = address +1)
11	If (address < 64) then 6
12	Reset $\overline{CSi}$ per fig. 1-13g
13	Increment chip select counter (i=i+1 and $\overline{CSi} = \overline{CSi+1}$)
14	If (i < 8) then 4
15	Increment read loop counter (J = J+1)
16	If (J < 9) then 3
17	Reset CL per fig. 1-13j
18	End Routine

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```
BORAM HYBRID MICROCIRCUIT FUNCTIONAL TEST

SERIAL #00014                    10 JAN 78

     CHIP  1  PASS        CHIP  2  PASS
     CHIP  3  PASS        CHIP  4  PASS
     CHIP  5  PASS        CHIP  6  PASS
     CHIP  7  PASS        CHIP  8  PASS
     CHIP  9  PASS        CHIP 10  PASS
     CHIP 11  PASS        CHIP 12  PASS
     CHIP 13  PASS        CHIP 14  PASS
     CHIP 15  PASS        CHIP 16  PASS


BORAM HYBRID MICROCIRCUIT FUNCTIONAL TEST

SERIAL #00015                    10 JAN 78

     CHIP  1  PASS        CHIP  2  PASS
     CHIP  3  PASS        CHIP  4  PASS
     CHIP  5  PASS        CHIP  6  ----
     CHIP  7  PASS        CHIP  8  PASS
     CHIP  9  PASS        CHIP 10  PASS
     CHIP 11  PASS        CHIP 12  PASS
     CHIP 13  PASS        CHIP 14  PASS
     CHIP 15  PASS        CHIP 16  PASS
```

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Figure 1-15. Sample Production Oriented Test Report

1-25

1.1.3.3 Engineering Report

A sample engineering oriented test report for two hybrid circuits appears in figure 1-16. This report presents the test results for each of 6 tests performed on each chip.

The engineering report is intended to allow a diagnosis of possible circuit problems to guide rework action. To use this tool the engineer or technician must be familiar with the nature of the individual tests.

As an example consider the results for chip 06 in hybrid 00015. This chip passed the counter pattern, erase recovery-checkerboard bar, zero pattern, one pattern, and read disturb tests. This implies that the chip functions properly. All wires must be in place, and all on chip circuitry must operate. The chip failed the erase recovery-checkerboard test. This implies that some memory transistor(s) are slow in recovery from multiple clearing. Thus in this case the rework action required is to replace the chip.

In other cases the combination of test results may indicate a wire bond problem, and detailed visual inspection would be called for.

1.1.3.4 Through Put Observations

The throughput capacity of the BORAM functional test station has been examined by formulating the sequence of actions an operator must perform, and by timing each individual action.

In this experiment, the actions were performed by engineers who had no significant previous experience with the detailed motions involved. Because the engineers lack the dexterity which would be aquired by a test operator, the observed times are believed to be pessimistic.

The scenario for a test operator involves two phases. A "start-up activity" sequence prepares the test system and the first group of eight hybrids for test. An "operating activity" maintains a continuous flow of hybrids through the test system by repeating a sequence of operations. It is assumed that the operator is continuously being given a supply of hybrids to be tested,

```
EDRAM HYBRID MICROCIRCUIT FUNCTIONAL TEST            10 JAN 70
Clear    1000 microsec              Write      300 microsec

SERIAL  CHIP   TEST    TEST    TEST    TEST    TEST    TEST    ALL
NUMBER  NUMBER #1      #2      #3      #4      #5      #6      TESTS

00014   01     PASS    PASS    PASS    PASS    PASS    PASS    PASS
00014   02     PASS    FASS    PASS    PASS    PASS    PASS    FASS
00014   03     PASS    PASS    PASS    PASS    PASS    PASS    PASS
00014   04     PASS    PASS    FASS    PASS    PASS    PASS    PASS
00014   05     PASS    PASS    PASS    PASS    PASS    PASS    PASS
00014   06     PASS    PASS    PASS    PASS    PASS    PASS    PASS
00014   07     PASS    PASS    PASS    PASS    PASS    PASS    PASS
00014   08     PASS    FASS    PASS    PASS    PASS    PASS    PASS
00014   09     PASS    FASS    PASS    PASS    PASS    PASS    PASS
00014   10     PASS    PASS    FASS    PASS    PASS    PASS    PASS
00014   11     PASS    FASS    PASS    PASS    PASS    PASS    PASS
00014   12     PASS    PASS    PASS    PASS    PASS    PASS    PASS
00014   13     PASS    PASS    PASS    PASS    PASS    PASS    PASS
00014   14     PASS    PASS    PASS    PASS    PASS    PASS    FASS
00014   15     PASS    PASS    PASS    PASS    PASS    PASS    PASS
00014   16     PASS    PASS    PASS    PASS    PASS    PASS    PASS
00015   01     PASS    PASS    FASS    PASS    PASS    PASS    PASS
00015   02     PASS    PASS    PASS    PASS    PASS    PASS    PASS
00015   03     PASS    PASS    PASS    PASS    PASS    PASS    PASS
00015   04     PASS    PASS    PASS    PASS    PASS    PASS    PASS
00015   05     PASS    PASS    PASS    PASS    PASS    PASS    PASS
00015   06     PASS    ----    PASS    PASS    PASS    PASS    ----
00015   07     PASS    PASS    FASS    PASS    PASS    PASS    PASS
00015   08     PASS    FASS    PASS    PASS    PASS    FASS    FASS
00015   09     PASS    PASS    PASS    PASS    PASS    PASS    PASS
00015   10     PASS    PASS    PASS    FASS    PASS    PASS    PASS
00015   11     PASS    PASS    PASS    FASS    PASS    PASS    PASS
00015   12     PASS    PASS    PASS    PASS    PASS    PASS    PASS
00015   13     PASS    PASS    PASS    PASS    PASS    FASS    FASS
00015   14     PASS    PASS    PASS    PASS    PASS    PASS    PASS
00015   15     PASS    PASS    PASS    PASS    PASS    PASS    PASS
00015   16     PASS    PASS    FASS    PASS    PASS    PASS    PASS
```

78-0332-VA-10

Figure 1-16. Sample Engineering Oriented Test Report

and that hybrids which have been tested are removed together with the test reports by other personnel.

A working assumption is that hybrids are brought to the test station in a container in groups of eight. The container also accommodates the routing ticket and other traveling manufacturing documentation. Each hybrid is labeled by a control number or serial number easily seen by the operator.

The operator's responsibility is to see that each hybrid is tested, and that the hybrids are returned to the proper container with the test reports. The serial numbers on the reports uniquely relate the data to the part.

To maintain a steady flow of product the operator must use both test channels. While channel A is engaged in testing eight hybrids, the operator must unload and reload channel B. Figure 1-17 shows this operating sequence and gives the times observed for each element. An operator should be able to cycle eight parts every seven minutes.
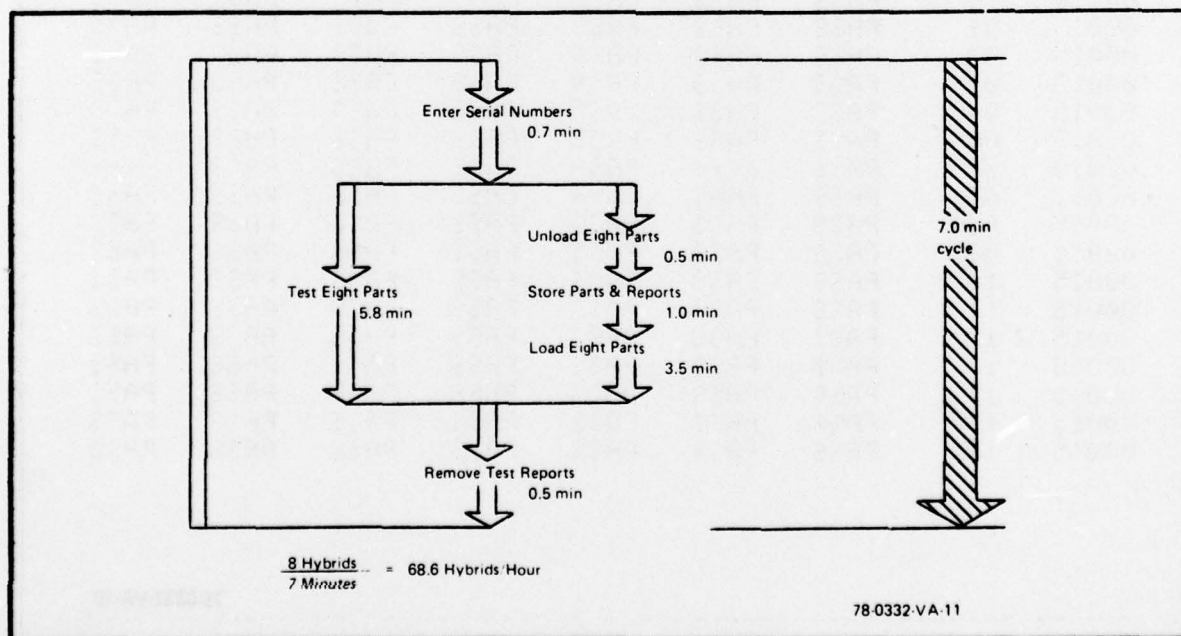

Figure 1-17. Sequence of Operations for the BORAM Functional Test

For the set of assumptions given this should be a comfortable working rate. In terms of hybrids per hour it amounts to 68.6. In paragraph 1.1.1.4, it was shown that an upper bound on the through put requirement was 62 hybrids per hour.

The setup activity was also examined. To prepare the test system about 0.5 minutes are required to insert the tape cartridge and load the test program. To run the initialization portion of the program takes 0.6 minutes. The initial loading of eight hybrids into test sockets takes about 3.5 minutes. The sum of these times is 4.6 minutes.

2. CONCLUSIONS

The development of the BORAM Function Test Station has solved the major electrical test "bottleneck" problem for the Manufacturing Methods Project. The concept of testing many hybrids simultaneously, and of oscillating between two test channels to hide the socket loading time, has allowed achievement of the necessary throughput capacity.

The magnitude of this achievement becomes more apparent when the capability of conventional automatic chip test systems is examined. A complete functional test of a BORAM die on a high speed test system normally takes more than one minute. If 128 chips were tested (and loading and unloading of the parts could be accomplished in zero time) approximately two hours of test time would be required. In other words, the BORAM Functional Test Station can process in seven minutes more circuits than a conventional automatic test system can do in two hours.

3. PROGRAM FOR NEXT INTERVAL

The primary task during the next period is the assembly of the confirmatory sample hybrids.

4. PUBLICATIONS AND REPORTS

During the reporting period there were no publications derived directly from this contract effort.

5. IDENTIFICATION OF TECHNICIANS

The following key engineers and management personnel were employed on the BORAM manufacturing methods project from July to December of 1977.

Technician	Manhours
J. Brewer	413
R. Popp	300
C. Walvogel	176
M. McKinnon	61

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